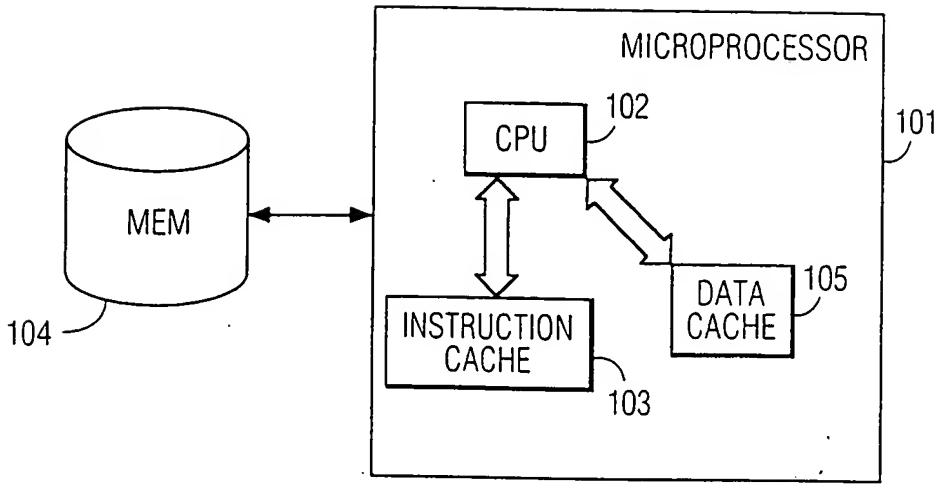

MICROPROCESSOR
101
CPU
102
MEM
104
INSTRUCTION CACHE
103
DATA CACHE
105

FIG. 1a

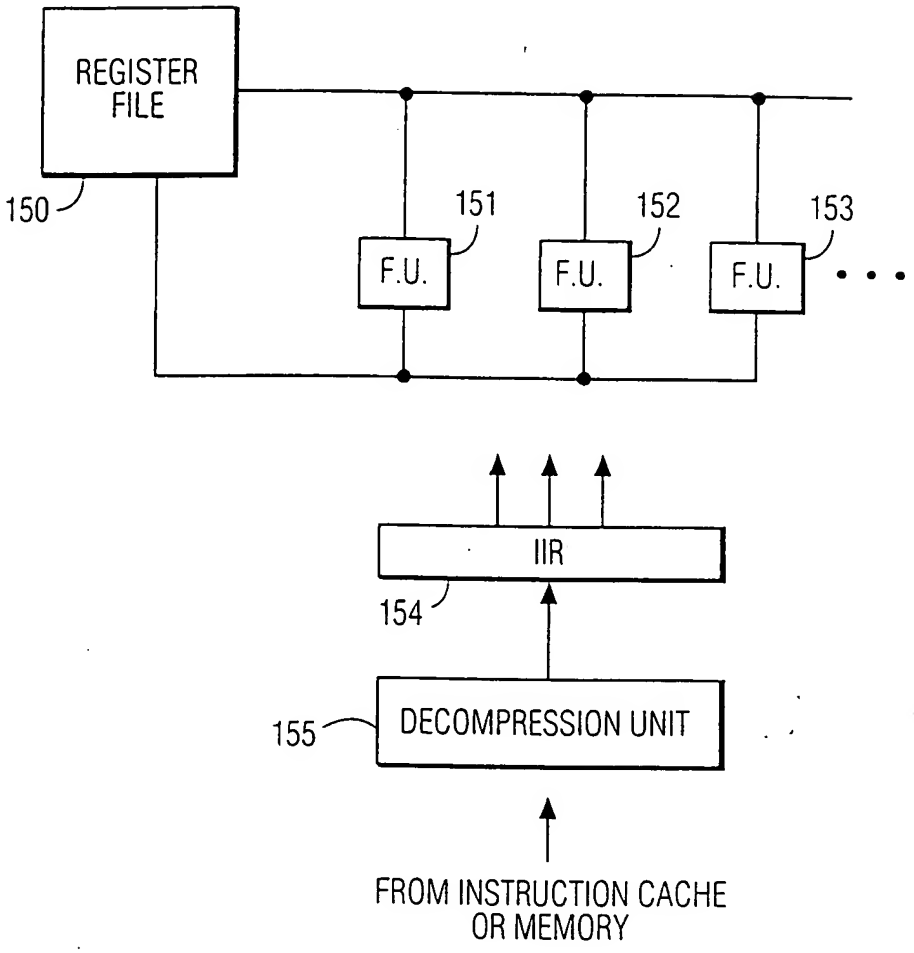

REGISTER FILE
150
151
152
153
F.U.
F.U.
F.U.
IIR
154
155
DECOMPRESSION UNIT
FROM INSTRUCTION CACHE OR MEMORY

FIG. 1b

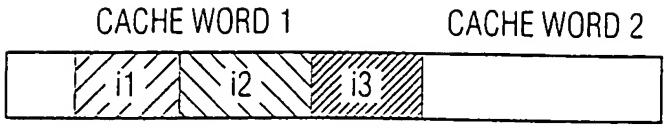


FIG. 2a

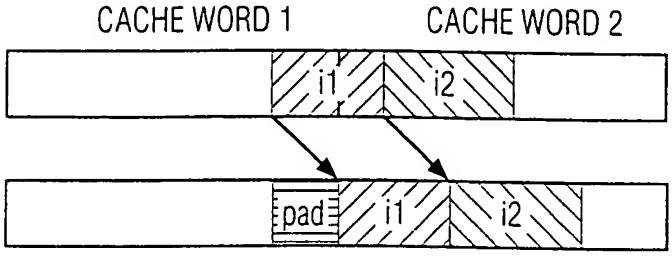


FIG. 2b

FIG. 2c

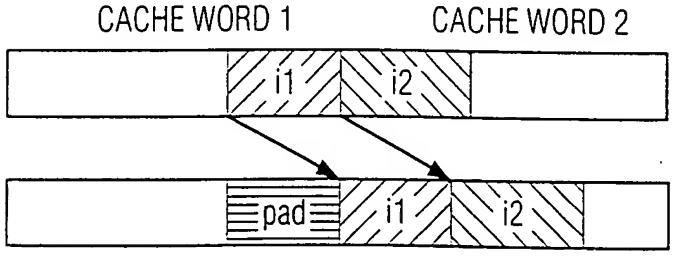
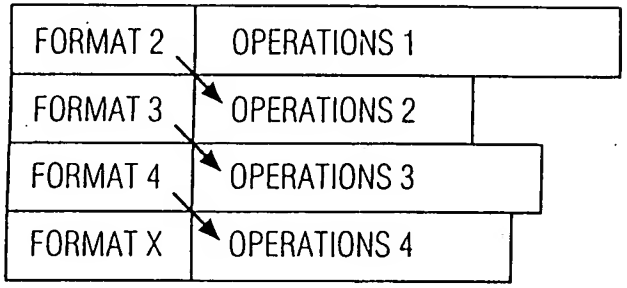


FIG. 2d

FIG. 2e



INSTRUCTION 1 - BRANCH TARGET, UNCOMPRESSED

INSTRUCTION 2 - COMPRESSED

INSTRUCTION 3 - COMPRESSED

INSTRUCTION 4 - COMPRESSED

FIG. 3

FIG. 4a

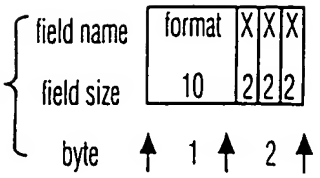


FIG. 4b

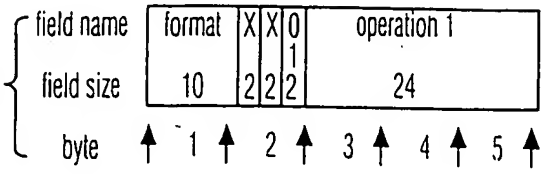


FIG. 4c

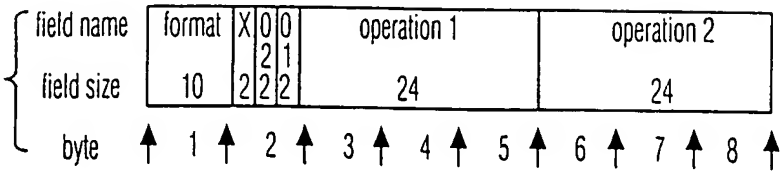


FIG. 4d

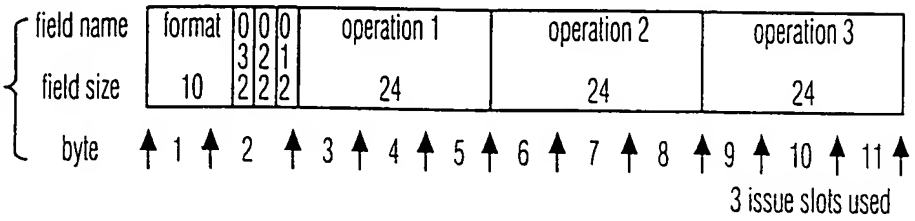


FIG. 4e

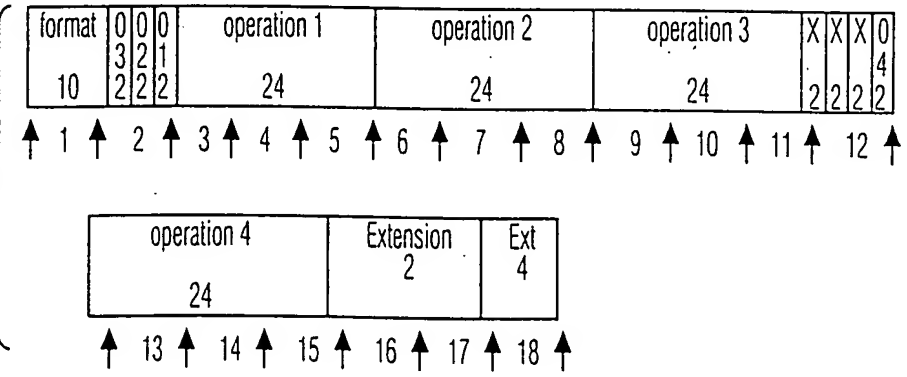
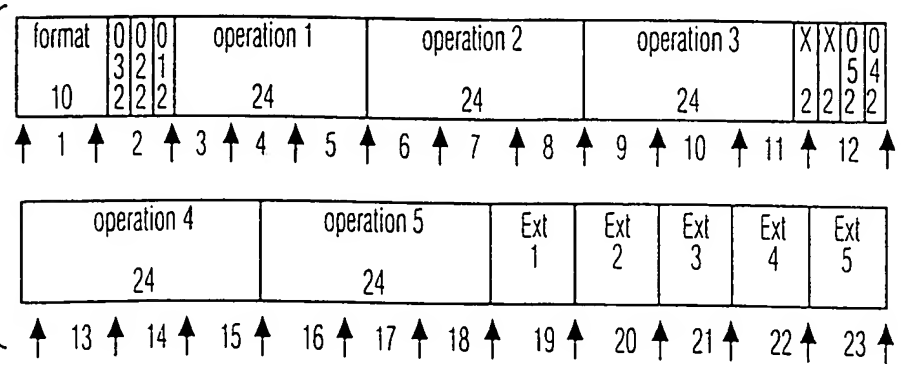


FIG. 4f



	24-bit operation part				2-bit part	Extension	Size
	bit position						
name	0-6	7-13	14-20	21-23	24-25	26-34-41	
26-format:							
<binary-unguarded-short>	src1[0:6]	src2[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]		26
<unary-param7-unguarded-short>	src1[0:6]	param[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]		26
<binary-unguarded-param7-resultless-short>	src1[0:6]	src2[0:6]	param[0:6]	opcode[0:2]	opcode[3:4]		26
<unary-short>	src1[0:6]	dst[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]		26
34-format:							
<binary-short> iadd,etc.	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	dst[0:6] 0	34
<unary-param-7-short>	src1[0:6]	param[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	dst[0:6] 0	34-
<binary-param7-resultless-short>	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	param [0:6] 0	34
<binary-unguarded>	src1[0:6]	src2[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]XL011	34
<binary-resultless>	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]X1001	34
<unary-param7-un-guarded>	src1[0:6]	param[0:6]	dst[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]SL111	34
<unary>	src1[0:6]	dst[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]XL101	34

FIG. 5a

42-format:							
<binary-param7-resultless>	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]SXX100param[0:6]	42
<binary>	src1[0:6]	src2[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]XL0101 dst[0:6]	42
<unary-param7>	src1[0:6]	param[0:6]	guard[0:6]	opcode[0:2]	opcode[3:4]	opcode[5:7]SL1101 dst[0:6]	42
<zeroary-param32>	param[7:13]	param[0:6]	dst[0:6]	param[14:16]	param[17:18]	param[19:23]XX1 param[24:31]	42
<zeroary-param32-resultless>	param[7:13]	param[0:6]	guard[0:6]	param[14:16]	param[17:18]	param[19:23]000 param[24:31]	42
<zeroary-param32-resultless>	param[7:13]	param[0:6]	guard[0:6]	param[14:16]	param[17:18]	param[19:23]100 param[24:31]	42

Note:
S: signed/unsigned format bit for parametric operations; S=1 if signed, S=0 if unsigned
L: latency format bit; L=0 if (latency=1 and this is not a resultless operation) else L=1
X: undefined value

FIG. 5b

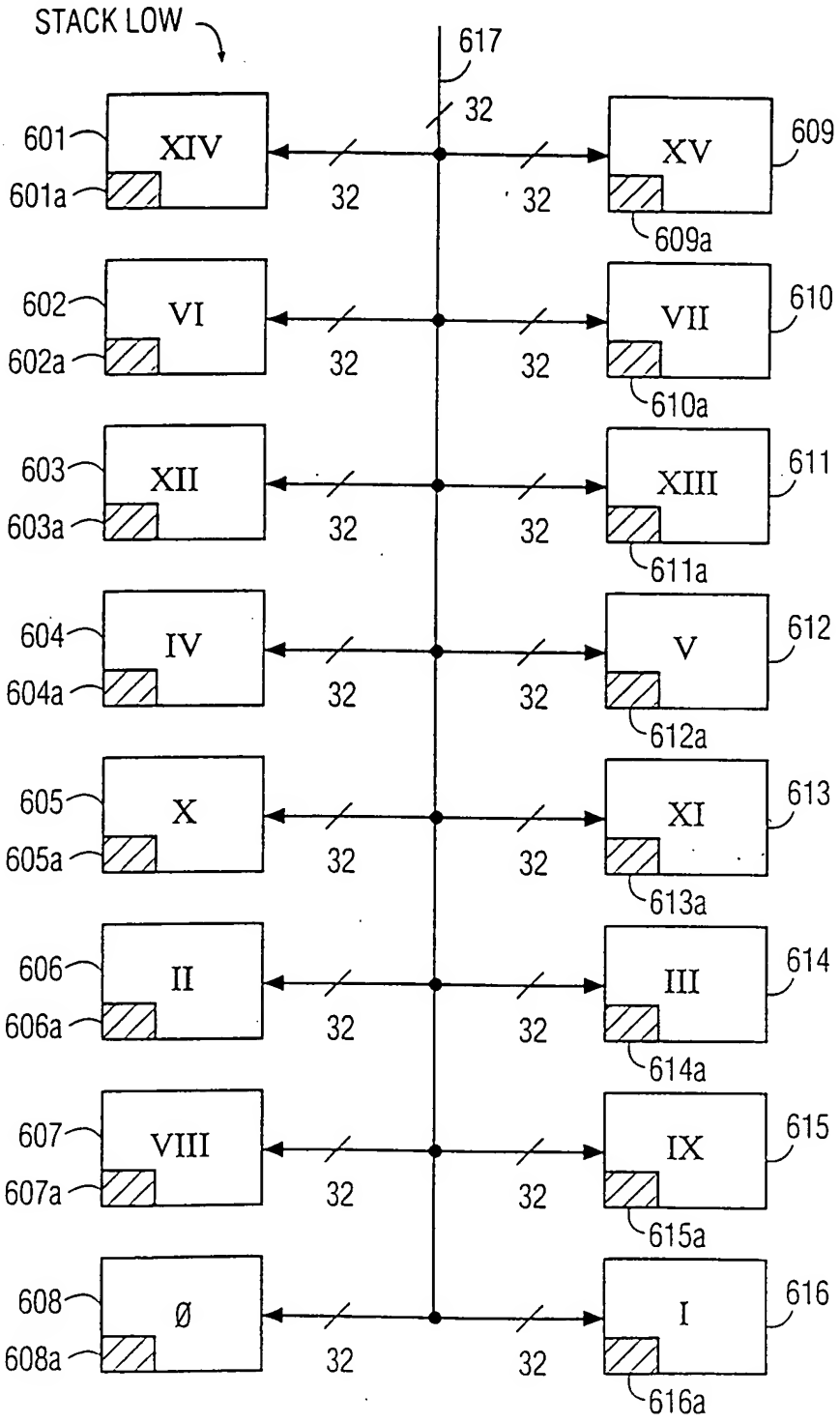

STACK LOW
617
32
601
XIV
601a
32
32
XV
609
609a
602
VI
602a
32
32
VII
610
610a
603
XII
603a
32
32
XIII
611
611a
604
IV
604a
32
32
V
612
612a
605
X
605a
32
32
XI
613
613a
606
II
606a
32
32
III
614
614a
607
VIII
607a
32
32
IX
615
615a
608
Ø
608a
32
32
I
616
616a

FIG. 6a

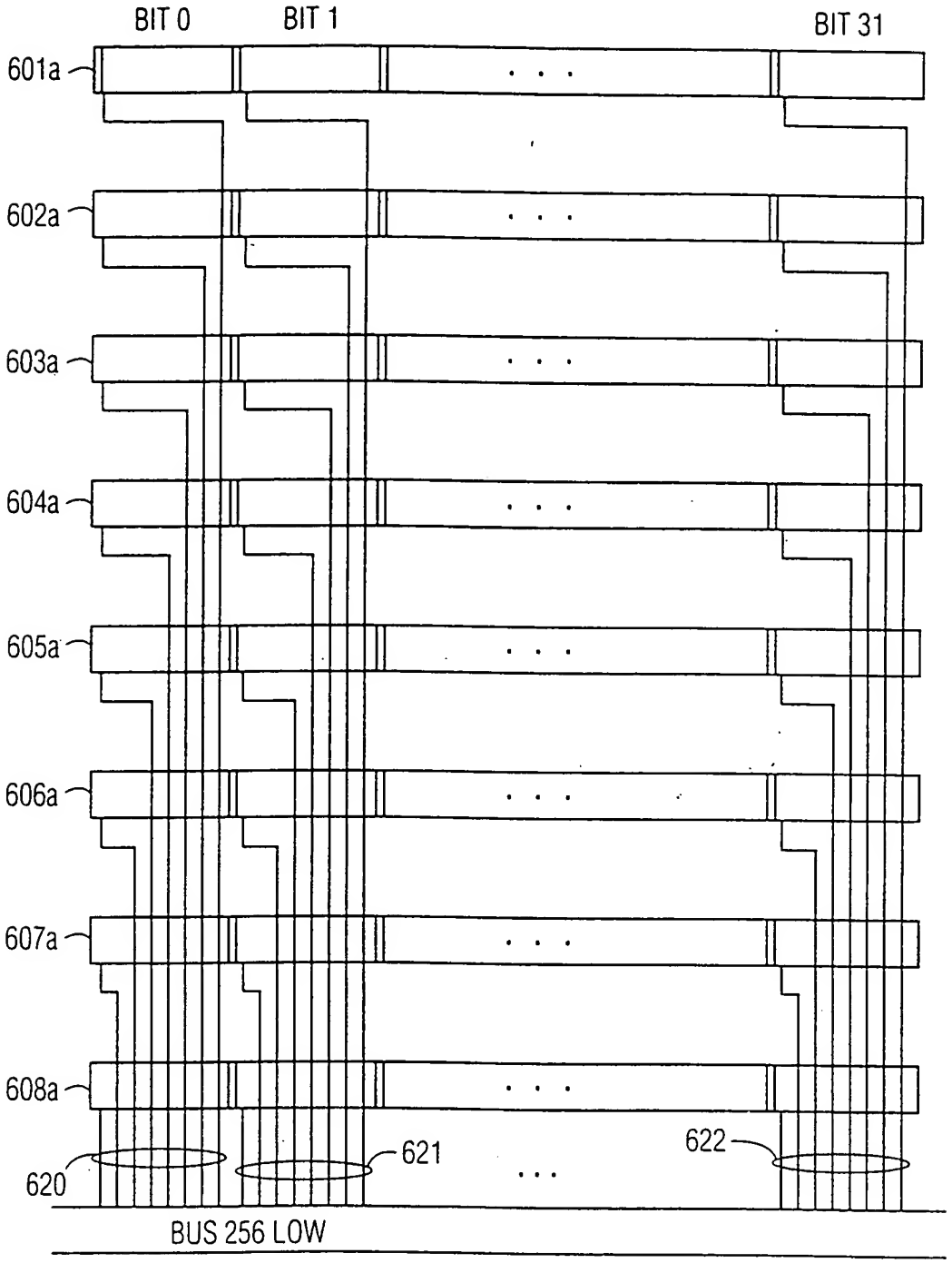

BIT 0
BIT 1
BIT 31
601a
602a
603a
604a
605a
606a
607a
608a
620
621
622
BUS 256 LOW

FIG. 6b

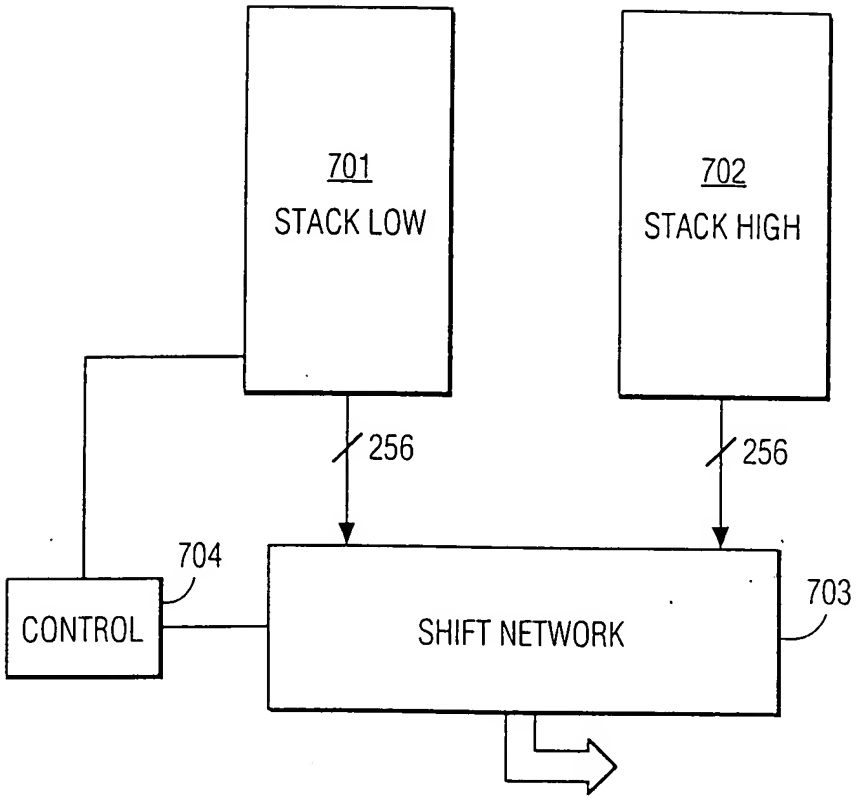

701
STACK LOW
702
STACK HIGH
256
256
704
CONTROL
SHIFT NETWORK
703

FIG. 7

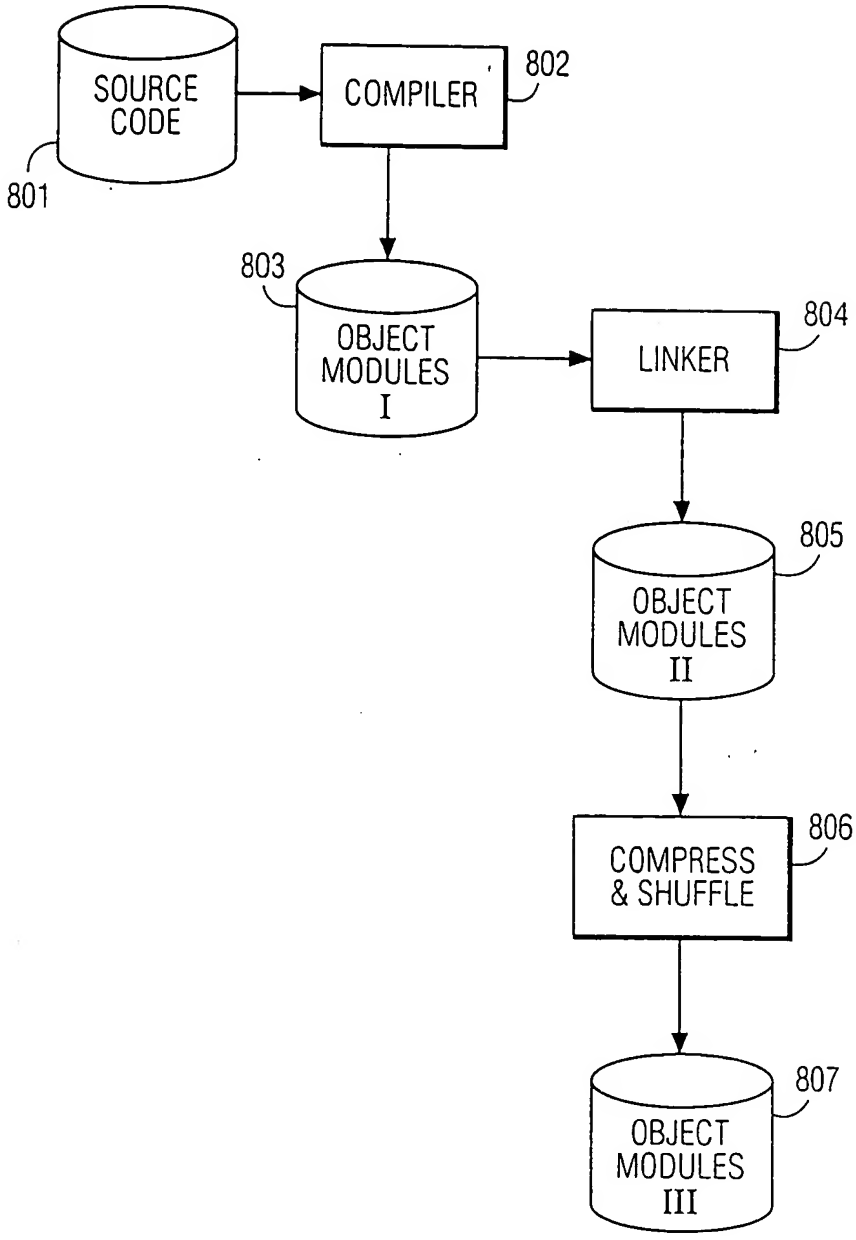

SOURCE CODE
801
COMPILER
802
803
OBJECT MODULES I
LINKER
804
OBJECT MODULES II
805
COMPRESS & SHUFFLE
806
OBJECT MODULES III
807

FIG. 8

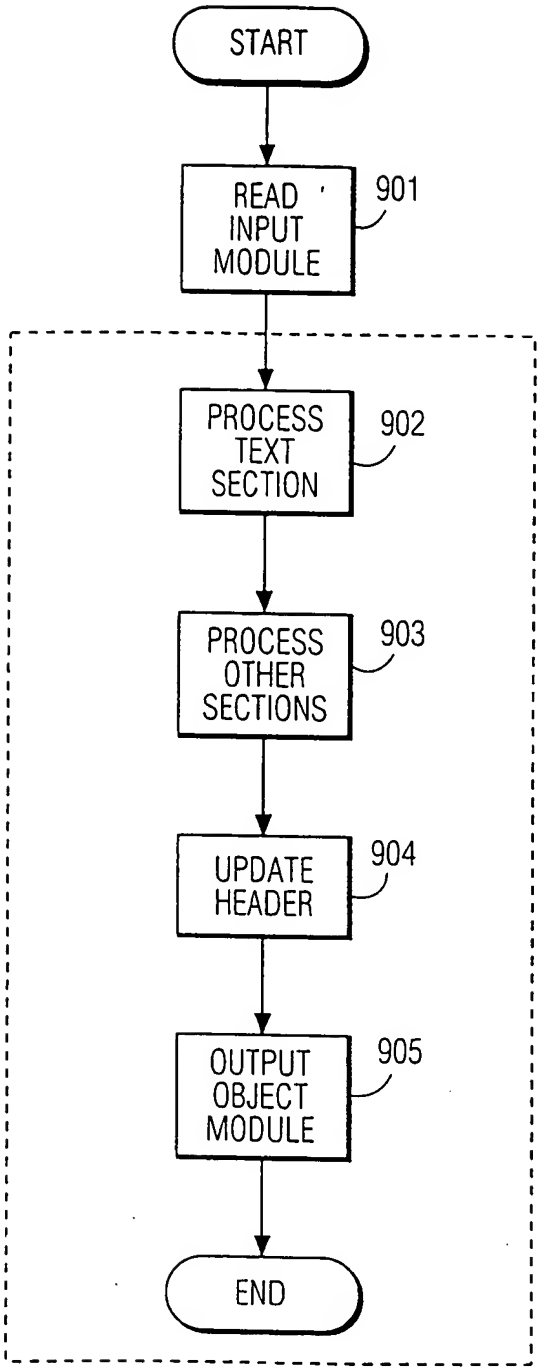

START
READ INPUT MODULE
901
PROCESS TEXT SECTION
902
PROCESS OTHER SECTIONS
903
UPDATE HEADER
904
OUTPUT OBJECT MODULE
905
END

FIG. 9

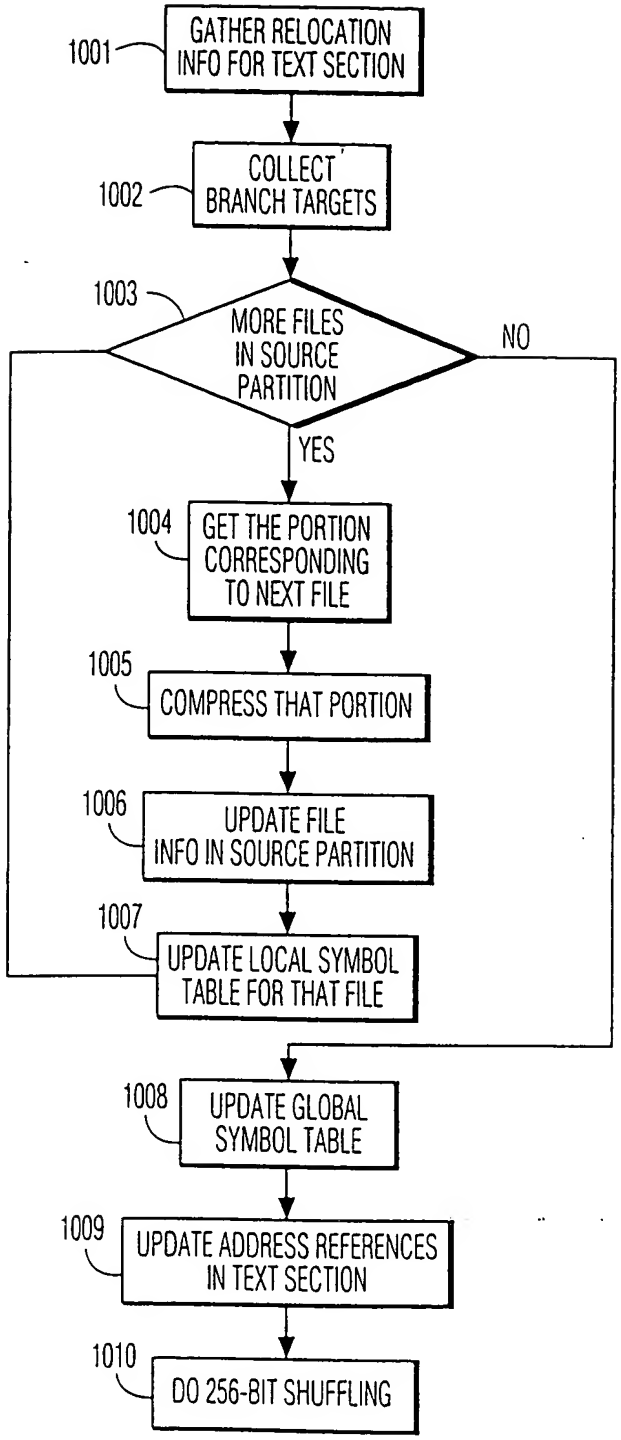

1001
GATHER RELOCATION INFO FOR TEXT SECTION
1002
COLLECT BRANCH TARGETS
1003
MORE FILES IN SOURCE PARTITION
NO
YES
1004
GET THE PORTION CORRESPONDING TO NEXT FILE
1005
COMPRESS THAT PORTION
1006
UPDATE FILE INFO IN SOURCE PARTITION
1007
UPDATE LOCAL SYMBOL TABLE FOR THAT FILE
1008
UPDATE GLOBAL SYMBOL TABLE
1009
UPDATE ADDRESS REFERENCES IN TEXT SECTION
1010
DO 256-BIT SHUFFLING

FIG. 10

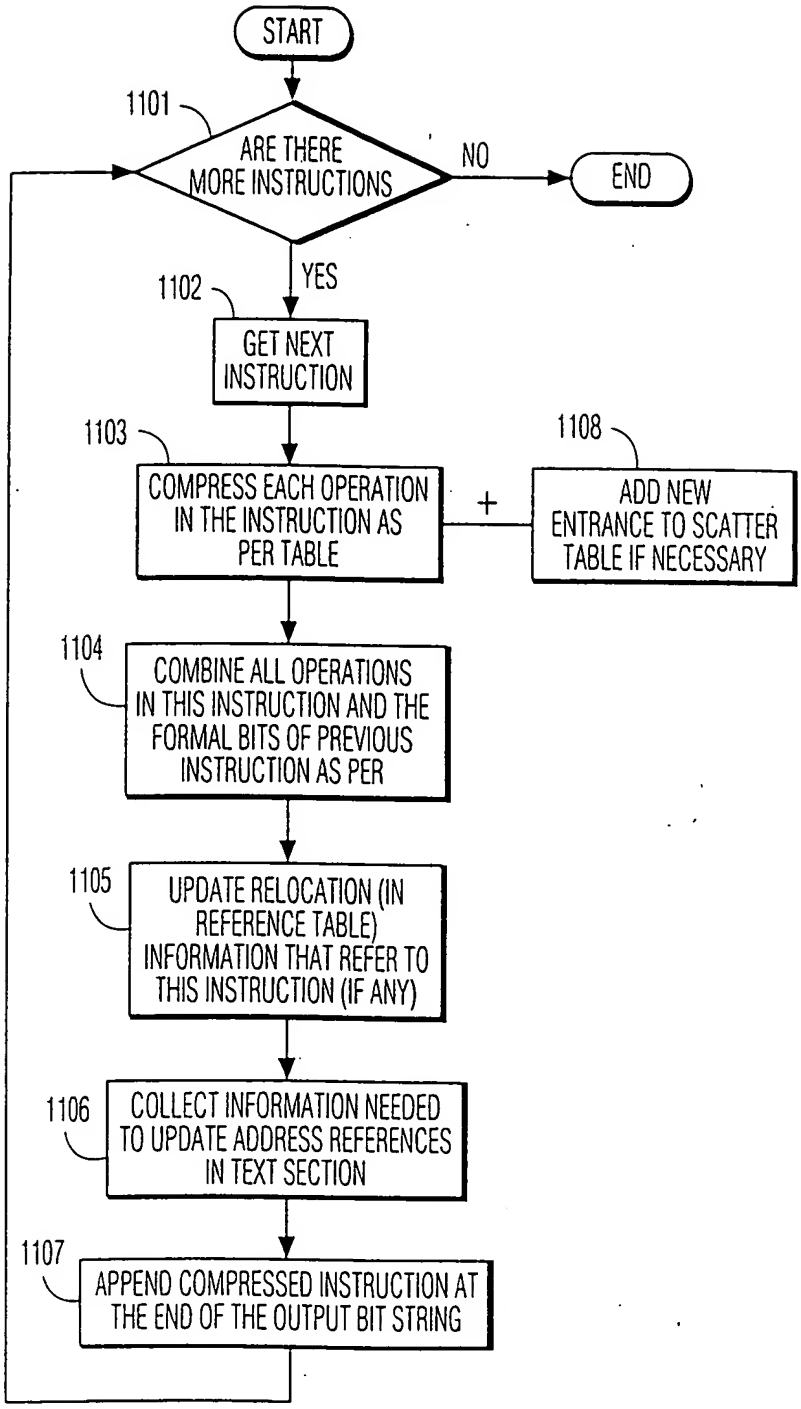

START
1101
ARE THERE MORE INSTRUCTIONS
NO
END
YES
1102
GET NEXT INSTRUCTION
1103
COMPRESS EACH OPERATION IN THE INSTRUCTION AS PER TABLE
+
1108
ADD NEW ENTRANCE TO SCATTER TABLE IF NECESSARY
1104
COMBINE ALL OPERATIONS IN THIS INSTRUCTION AND THE FORMAL BITS OF PREVIOUS INSTRUCTION AS PER
1105
UPDATE RELOCATION (IN REFERENCE TABLE) INFORMATION THAT REFER TO THIS INSTRUCTION (IF ANY)
1106
COLLECT INFORMATION NEEDED TO UPDATE ADDRESS REFERENCES IN TEXT SECTION
1107
APPEND COMPRESSED INSTRUCTION AT THE END OF THE OUTPUT BIT STRING

FIG. 11

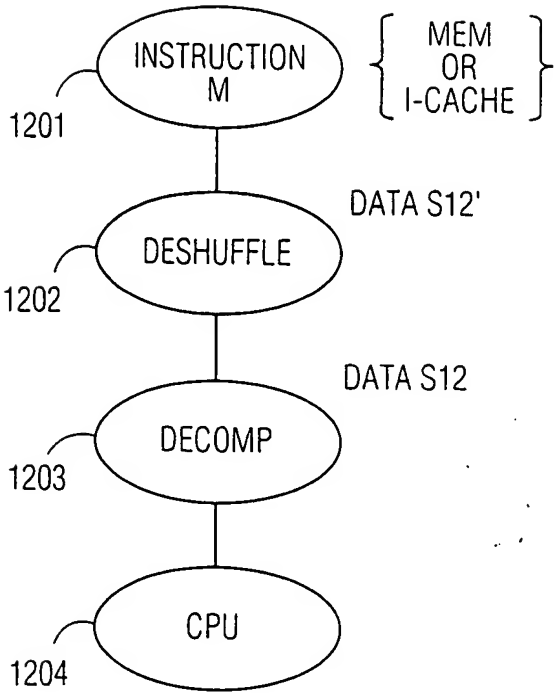

INSTRUCTION
M
MEM
OR
I-CACHE
1201
DATA S12'
DESHUFFLE
1202
DATA S12
DECOMP
1203
CPU
1204

FIG. 12